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**//BCD to 7 segment display ///**

module seven\_seg(a,b,c,d,e,f,g,A,B,C,D

);

output a,b,c,d,e,f,g;

input A,B,C,D;

wire y\_D,y\_B,y\_C,y\_A;

wire y\_a31,y\_a32,y\_a21,y\_a22,y\_a23,y\_a24,y\_a33,y\_a34;

wire y\_b31,y\_b32,y\_b33,y\_b21,y\_b22,y\_b34,y\_b23;

wire y\_c21,y\_c22,y\_c23,y\_c24,y\_c25,y\_c31,y\_c26;

wire y\_d31,y\_d32,y\_d33,y\_d34,y\_d21,y\_d35,y\_d22;

wire y\_e21,y\_e22,y\_e23,y\_e24,y\_e25,y\_e26;

wire y\_f31,y\_f21,y\_f22,y\_f23,y\_f24,y\_f32,y\_f25;

wire y\_g31,y\_g21,y\_g22,y\_g23,y\_g24,y\_g32,y\_g25;

inv i1(y\_D,D);

inv i2(y\_C,C);

inv i3(y\_B,B);

inv i4(y\_A,A);

and3 a1(y\_a31,A,y\_B,y\_C);

and3 a2(y\_a32,y\_A,B,D);

and2 a3(y\_a21,y\_B,y\_D);

and2 a4(y\_a22,y\_A,C);

and2 a5(y\_a23,A,y\_D);

and2 a6(y\_a24,B,C);

or3 a7(y\_a33,y\_a31,y\_a32,y\_a21);

or3 a8(y\_a34,y\_a22,y\_a23,y\_a24);

or2 a9(a,y\_a33,y\_a34);

and3 b1(y\_b31,y\_A,y\_C,y\_D);

and3 b2(y\_b32,y\_A,C,D);

and3 b3(y\_b33,A,y\_C,D);

and2 b4(y\_b21,y\_B,y\_C);

and2 b5(y\_b22,y\_B,y\_D);

or3 b6(y\_b34,y\_b31,y\_b32,y\_b33);

or2 b7(y\_b23,y\_b21,y\_b22);

or2 b8(b,y\_b34,y\_b23);

and2 c1(y\_c21,y\_A,y\_C);

and2 c2(y\_c22,y\_A,D);

and2 c3(y\_c23,y\_C,D);

and2 c4(y\_c24,y\_A,B);

and2 c5(y\_c25,A,y\_B);

or3 c6(y\_c31,y\_c21,y\_c22,y\_c23);

or2 c7(y\_c26,y\_c24,y\_c25);

or2 c8(c,y\_c31,y\_c26);

and3 d1(y\_d31,y\_A,y\_B,y\_D);

and3 d2(y\_d32,y\_B,C,D);

and3 d3(y\_d33,B,y\_C,D);

and3 d4(y\_d34,B,C,y\_D);

and2 d5(y\_d21,A,y\_C);

or3 d6(y\_d35,y\_d31,y\_d32,y\_d33);

or2 d7(y\_d22,y\_d34,y\_d21);

or2 d8(c,y\_d35,y\_d22);

and2 e1(y\_e21,A,C);

and2 e2(y\_e22,A,B);

and2 e3(y\_e23,C,y\_D);

and2 e4(y\_e24,y\_B,y\_D);

or2 e5(y\_e25,y\_e21,y\_e22);

or2 e5(y\_e26,y\_e23,y\_e24);

or2 e6(e,y\_e25,y\_e26);

and3 f1(y\_f31,y\_A,B,y\_C);

and2 f2(y\_f21,y\_C,y\_D);

and2 f3(y\_f22,B,y\_D);

and2 f4(y\_f23,A,y\_B);

and2 f5(y\_f24,A,C);

or3 f6(y\_f32,y\_f31,y\_f21,y\_f22);

or2 f7(y\_f25,y\_f23,y\_f24);

or2 f8(f,y\_f32,y\_f25);

and3 g1(y\_g31,y\_A,B,y\_C);

and2 g2(y\_g21,A,y\_B);

and2 g3(y\_g22,A,D);

and2 g4(y\_g23,y\_B,C);

and2 g5(y\_g24,C,y\_D);

or3 g6(y\_g32,y\_g31,y\_g21,y\_g22);

or2 g7(y\_g25,y\_g23,y\_g24);

or2 g8(g,y\_g32,y\_g25);

endmodule

**//inverter using CMOS**

module inv(Y,A);

output Y;

input A;

supply0 gnd;

supply1 vdd;

pmos p1(Y,vdd,A);

nmos n1(Y,gnd,A);

endmodule

**// 3-input AND gate using CMOS**

module and3(Y, A, B, C);

output Y;

input A, B, C;

supply0 gnd;

supply1 vdd;

wire a, b;

pmos p1(a, vdd, A);

pmos p2(b, a, B);

pmos p3(Y, b, C);

nmos n1(Y, gnd, A);

nmos n2(Y, gnd, B);

nmos n3(Y, gnd, C);

endmodule

**// 2-input AND gate using CMOS**

module and2(Y, A, B);

output Y;

input A, B;

supply0 gnd;

supply1 vdd;

wire a;

pmos p1(a, vdd, A);

pmos p2(Y, a, B);

nmos n1(Y, gnd, A);

nmos n2(Y, gnd, B);

endmodule

**// 3-input OR gate using CMOS**

module or3(Y, A, B, C);

output Y;

input A, B, C;

supply0 gnd;

supply1 vdd;

wire a, b;

pmos p1(a, vdd, A);

pmos p2(b, vdd, B);

pmos p3(Y, vdd, C);

nmos n1(Y, gnd, A);

nmos n2(Y, gnd, B);

nmos n3(Y, gnd, C);

endmodule

**// 2-input OR gate using CMOS**

module or2(Y, A, B);

output Y;

input A, B;

supply0 gnd;

supply1 vdd;

wire a;

pmos p1(a, vdd, A);

pmos p2(Y, a, B);

nmos n1(Y, gnd, A);

nmos n2(Y, gnd, B);

endmodule

**//BCD to 7 segment**

module segment7(

bcd,

seg

);

input [3:0] bcd;

output [6:0] seg;

reg [6:0] seg;

always @(bcd)

begin

case (bcd)

0 : seg = 7'b0000001;

1 : seg = 7'b1001111;

2 : seg = 7'b0010010;

3 : seg = 7'b0000110;

4 : seg = 7'b1001100;

5 : seg = 7'b0100100;

6 : seg = 7'b0100000;

7 : seg = 7'b0001111;

8 : seg = 7'b0000000;

9 : seg = 7'b0000100;

default : seg = 7'b1111111;

endcase

end

endmodule